WHAT IS CLAIMED IS:

1. A method of generating multiple scrambling codes in a communication system, in which each of a plurality of base stations uses one of a plurality of primary scrambling codes and one of a plurality of secondary scrambling code sets each having a plurality of secondary scrambling codes, comprising:

setting an initial value of a scrambling code generator to a binary value of "n" when a n-th one of the plurality of primary scrambling codes is to be generated from the scrambling code generator to generate a desired primary scrambling code; and

setting an initial value of the scrambling code generator with a value obtained by shifting the n-th primary scrambling code by m times to generate a secondary scrambling code.

2. The method of claim 1, wherein the initial value of the scrambling code generator is set by setting a 7-th and 11-th bits included in the initial value to a value of 1, setting a first through 10-th bits, except for the 7-th and 11-th bits, to an 8 bit binary expression of "n," and setting remaining ones of the bits, other than the first through 11-th bits, to a value of "0".

3. A method of generating multiple scrambling codes, comprising:

generating a plurality of primary scrambling codes;

for each of the plurality of primary scrambling codes, generating a plurality of secondary scrambling codes by shifting the selected primary scrambling code by prescribed numbers of times;

comparing each of the plurality of primary scrambling codes to an initial value of each of the secondary scrambling codes; and

discarding each one of the primary scrambling codes that has a value equal to the secondary scrambling codes.

4. A forward multiple scrambling code generating apparatus, comprising:

a first shift register, which shifts bits of a bit stream by one bit in response to every input of an external unit clock, respectively, and outputs data for the generation of a primary scrambling code;

a second shift register, which shifts bits of a bit stream by one bit in response to every input of an external unit clock, respectively, and outputs data for the generation of the primary scrambling code and a secondary scrambling code;

a masking function unit, which receives respective outputs from the first and second shift registers, and performs a masking function for the received data to output data for the generation of the secondary scrambling code, wherein the primary scrambling

code is generated by performing a binary addition of the output from the second shift register to an output from the first shift register, and the secondary scrambling code is generated by performing a binary addition of the output from the masking function unit to the output from the second shift register.

5. The apparatus of claim 4, wherein the first shift register comprises an 18 bit register, in which a value obtained after a binary addition of an output of a 0-th one of the 18 bits to an output of a 7-th one of the 18 bits is fed back to a 17-th one of the 18 bits.

6. The apparatus of claim 4, wherein the second shift register comprises an 18 bit register, in which a value obtained after a binary addition of outputs from a 0-th, 5-th, 7-th, and 10-th one of the 18 bits is fed back to a 17-th one of the 18 bits.

7. A code generating apparatus, comprising:

a first shift register, which outputs a first register output;

a second shift register, which outputs a second register output; and

a masking function unit, coupled to receive the first and second register outputs, and output a masking output, wherein the first register output and the second register output are combined to generate a primary scrambling code, and the second

register output and the masking output are combined to generate a secondary scrambling code.

8. The apparatus of claim 7, wherein the first register output and the second register output are combined using binary addition, and the second register output and the masking output are combined using binary addition.

9. The apparatus of claim 7, wherein the first register output is generated by logically combing selected bits of the first shift register and feeding a result back to a prescribed bit of the first shift register.

10. The apparatus of claim 9, wherein the first shift register comprises an 18 bit register, and wherein the selected bits comprise a 0-th and seventh one of the 18 bits and the prescribed bit is a 17-th one of the 18 bits.

11. The apparatus of claim 7, wherein the second register output is generated by logically combing selected bits of the second shift register and feeding a result back to a prescribed bit of the second shift register.

12. The apparatus of claim 11, wherein the second shift register comprises an 18 bit register, and wherein the selected bits comprise a 0-th, 5-th, 7-th, and 10-th one of the 18 bits, and the prescribed bit comprises a 17-th one of the 18 bits.

13. The apparatus of claim 7, wherein an initial value of an n-th secondary scrambling code of an m-th secondary scrambling code set is generated using a value obtained after shifting an n-th primary scrambling code by m times.

14. A method of generating multiple scrambling codes in a communication system, comprising:

generating a primary scrambling code by setting an initial value of a scrambling code to a binary value of "n" when a n-th one of the plurality of primary scrambling codes is to be generated; and

generating an n-th secondary scrambling code set corresponding to the n-th primary scrambling code by shifting the n-th primary scrambling code by each of 0 through M times, wherein M is a number of secondary codes in the secondary code set.

15. The method of claim 14, wherein the initial value of the primary scrambling code is set by setting a 7-th and 11-th bit included in the initial value to a value of 1, setting a first through 10-th bits, except for the 7-th and 11-th bits, to a binary expression

of "n" consisting of different 8 bits, respectively, and setting remaining ones of the bits, other than the first through 11-th bits, to a value of "0".

16. The method of claim 14, wherein the step of setting the initial value for the scrambling code generator further comprises:

(a) setting a plurality of temporal primary scrambling codes, the number of the temporal primary scrambling codes being more than the number of the primary scrambling codes;

(b) setting the initial value, adapted to generate a n-th one of the temporal primary scrambling codes, with a value of "n";

(c) calculating respective initial values, adapted to generate the secondary scrambling codes in the first one of the secondary scrambling code set, based on the value of "n";

(d) detecting each secondary scrambling code in a secondary scrambling code set that have the same initial value as one of the temporal primary scrambling codes, based on the set and calculated initial values;

(e) discarding the j-th temporal primary scrambling code or a i-th one of the temporal primary scrambling codes when the initial value of an i-th one of the secondary scrambling codes corresponds to that of a j-th one of the temporal primary scrambling codes;

(f) repeatedly executing steps (b) through (e) up to an M-th one of the secondary scrambling code sets; and

(g) selecting as the primary scrambling codes N codes from the remaining temporal primary scrambling codes after executing step (d) for the M-th secondary scrambling code set, and when a j-th one of the finally left temporal primary scrambling codes is selected as an n-th one of the primary scrambling codes, mapping the values of "n" and "j", thereby setting the value of "j" as an initial value adapted to generate the n-th primary scrambling code.